HCAL Front End Electronics

H C A L

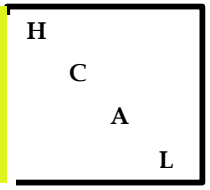
Theresa Shaw

CMS HCAL Electronics Project Engineer

DOE/NSF Review

May 9, 2001

Front End Electronics



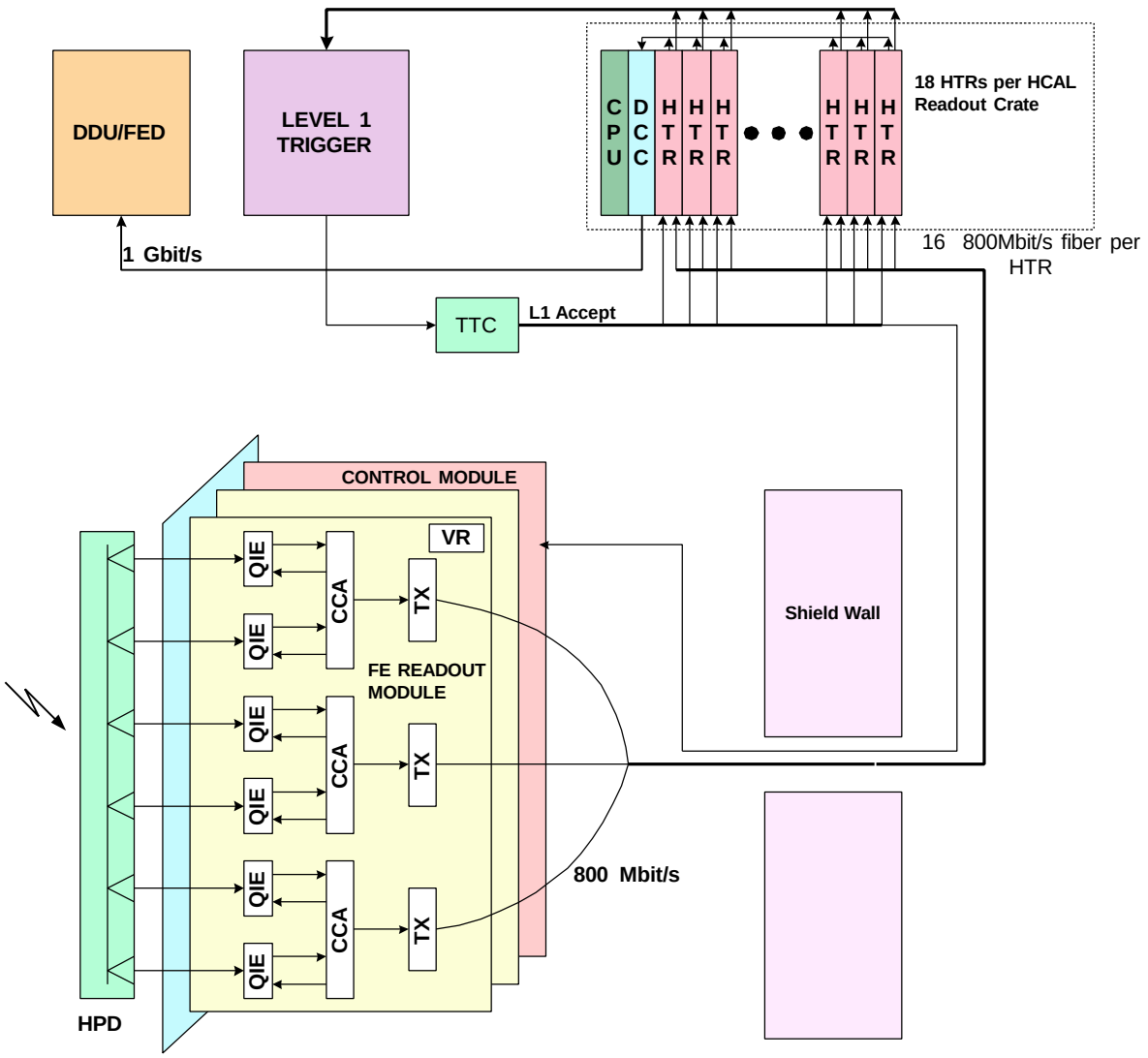
Electronics

- Scope
- System Overview
- Power/Packaging
- Backplanes
- Readout Cards
- ASICs
- Production Schedule

Front End System

System	Channel Count	Base Cost
2.1.5 HB	5040	442K
2.2.5 HO	2556	297K
2.3.5 HE	3744	409K
2.5.5 HF	2412	424K
Develop		2446K
Spares		392K
2.x.5	13752	4410K

FE/DAQ Readout



FE crates

HB, HE and HO make use of a custom Readout BoX (RBX)

HF will use standard Eurocard Packaging

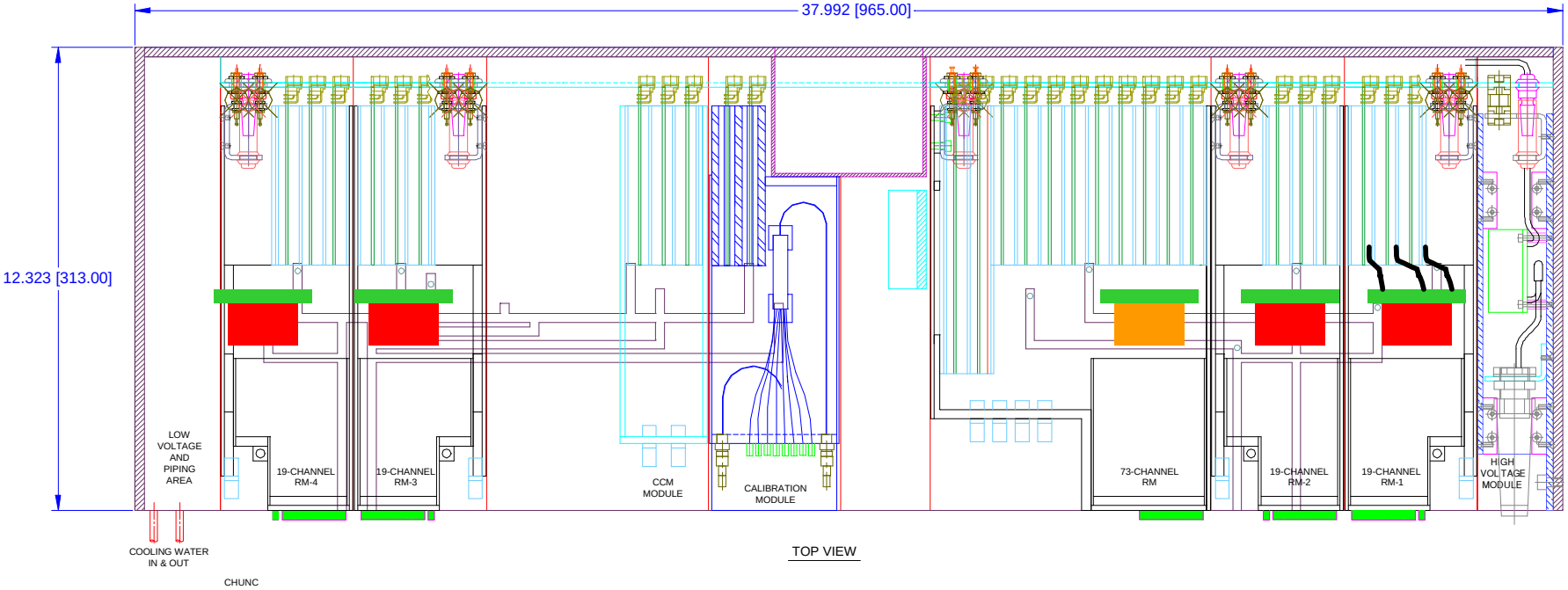
Crates Provide

- **Power,**
- **Cooling,**
- **Backplanes**

HB RBX

36 HB RBXs

4968 Channels



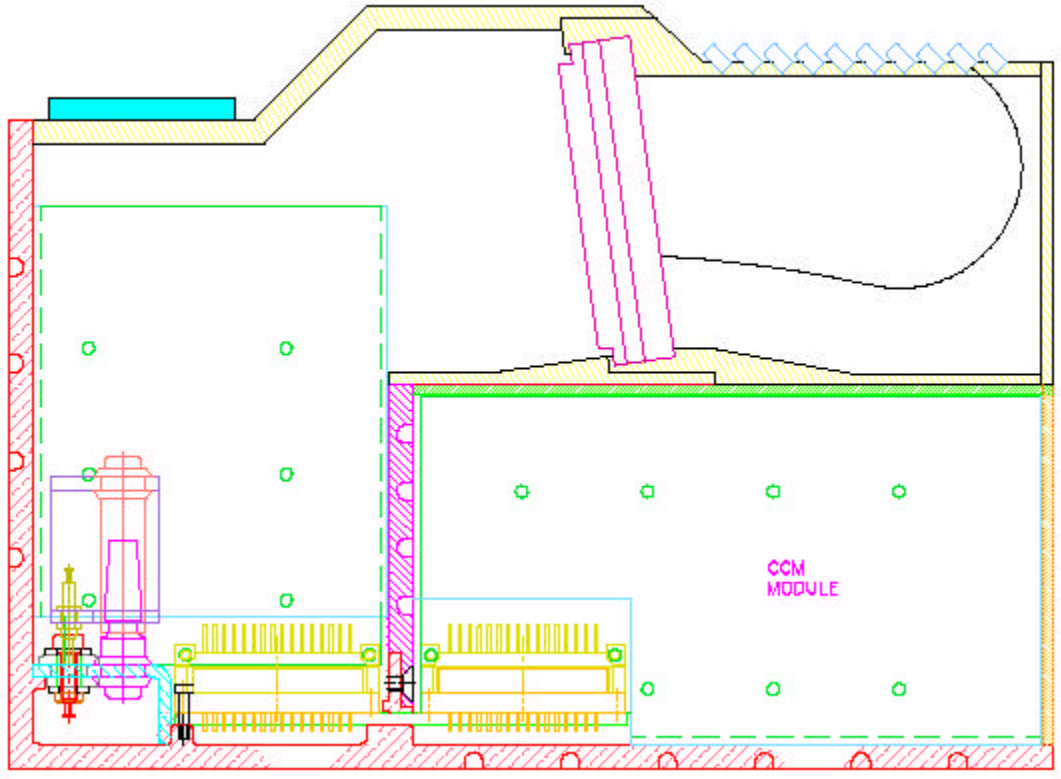
HB RBX COMPOSITE ASSEMBLY DRAWING

R. FOLTZ, FERMI LAB
J. MARCHANT, UNIV. OF NOTRE DAME
AS OF 23 FEBRUARY 2001

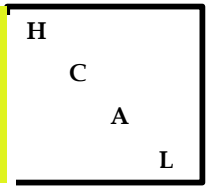
HE Box

36 HE RBXs

3672 Channels



Power Consumption



Power Consumption

HB – 298 W
23A@6.5V
33A@4.5V

HE – 205 W
17A@6.5V
21A@4.5V

HO+/- – 135 W
10A@6.5V
15A@4.5V

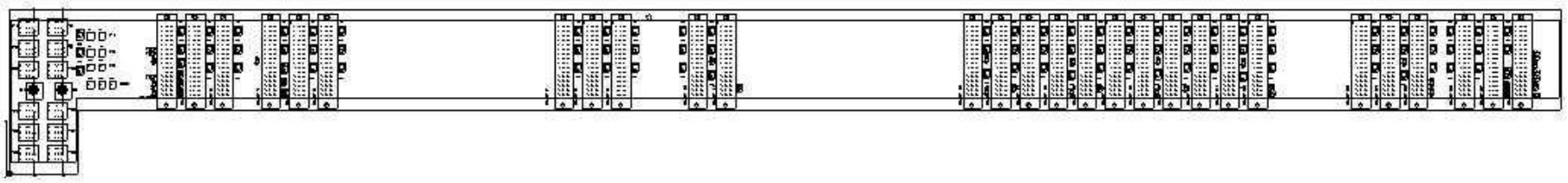
HO-0 – 189 W
16A@6.5V
21A@4.5V

			CURRENT and POWER at BOARD LEVEL										
FE Boards	QTY/BRD			POWER CONSUPTION					IDLING CURRENT				**TOTAL**
		VOLTAGE	5	5	2.5	3.3		5	5	2.5	3.3		
Chips													
QIE	6		0.2	0.4									
CCA	3					0.3							
Serializer	3				0.5								
LV regulat	3							0.025	0.025		0.025		
Current / Board			0.265	0.505		0.897727							
Total Power / Board													**9.044773**
Calibration Module		(There are two boards per module)											
		VOLTAGE	5	5	2.5	3.3		5	5	2.5	3.3		
Chips													
QIE	3		0.2	0.4									
CCA	3					0.3							
Serializer	2				0.5								
LV regulat	3							0.025	0.025		0.025		
Current / Module			0.145	0.265		0.697727							
Total Power / Module													**5.804773**
CCM													
		VOLTAGE				3.3							
Chips						5							
LV regulators													
Current / Board						1.515152							
Total Power / Board													**6.818182**

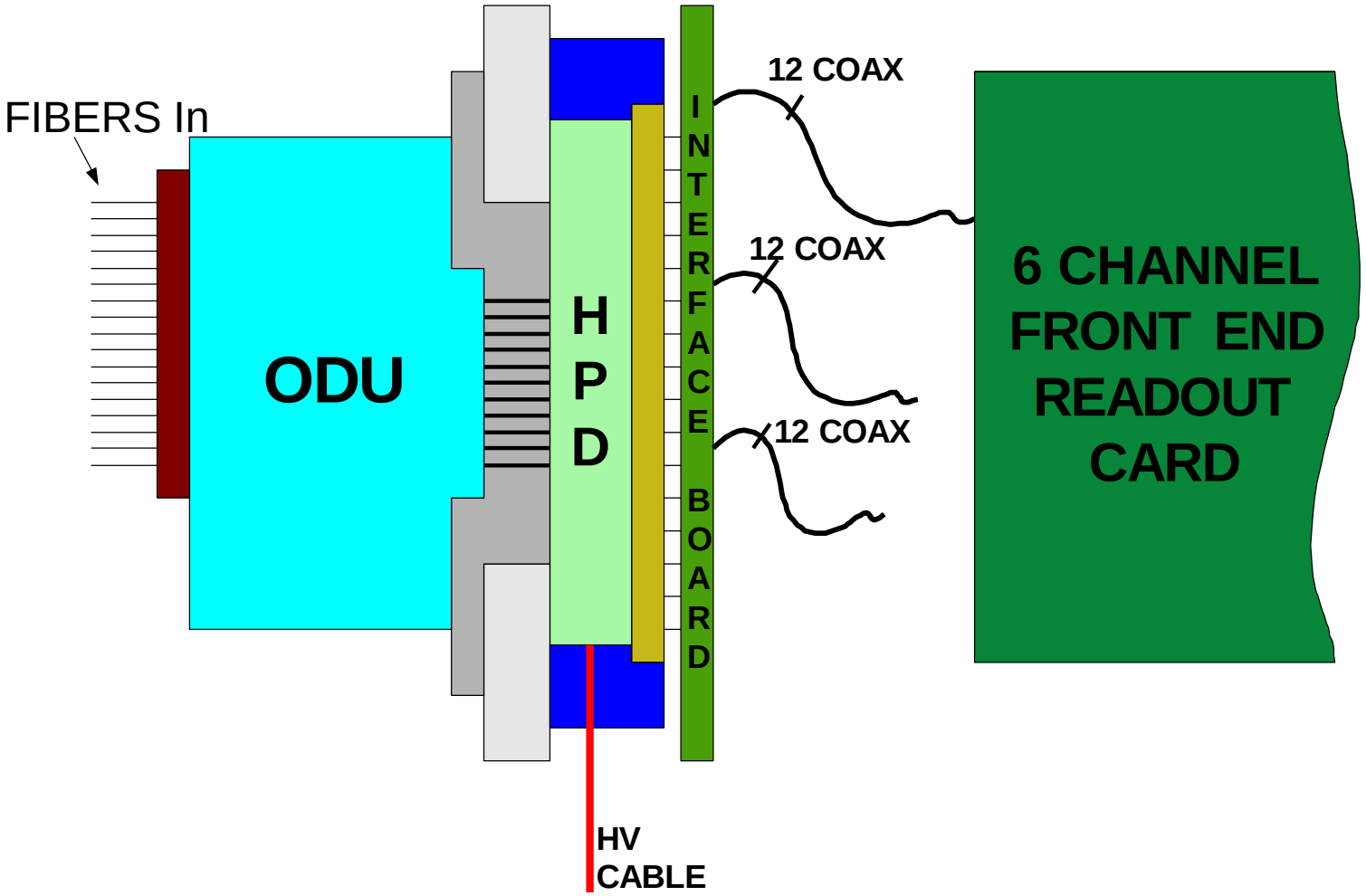
HB Backplane Function

Backplanes

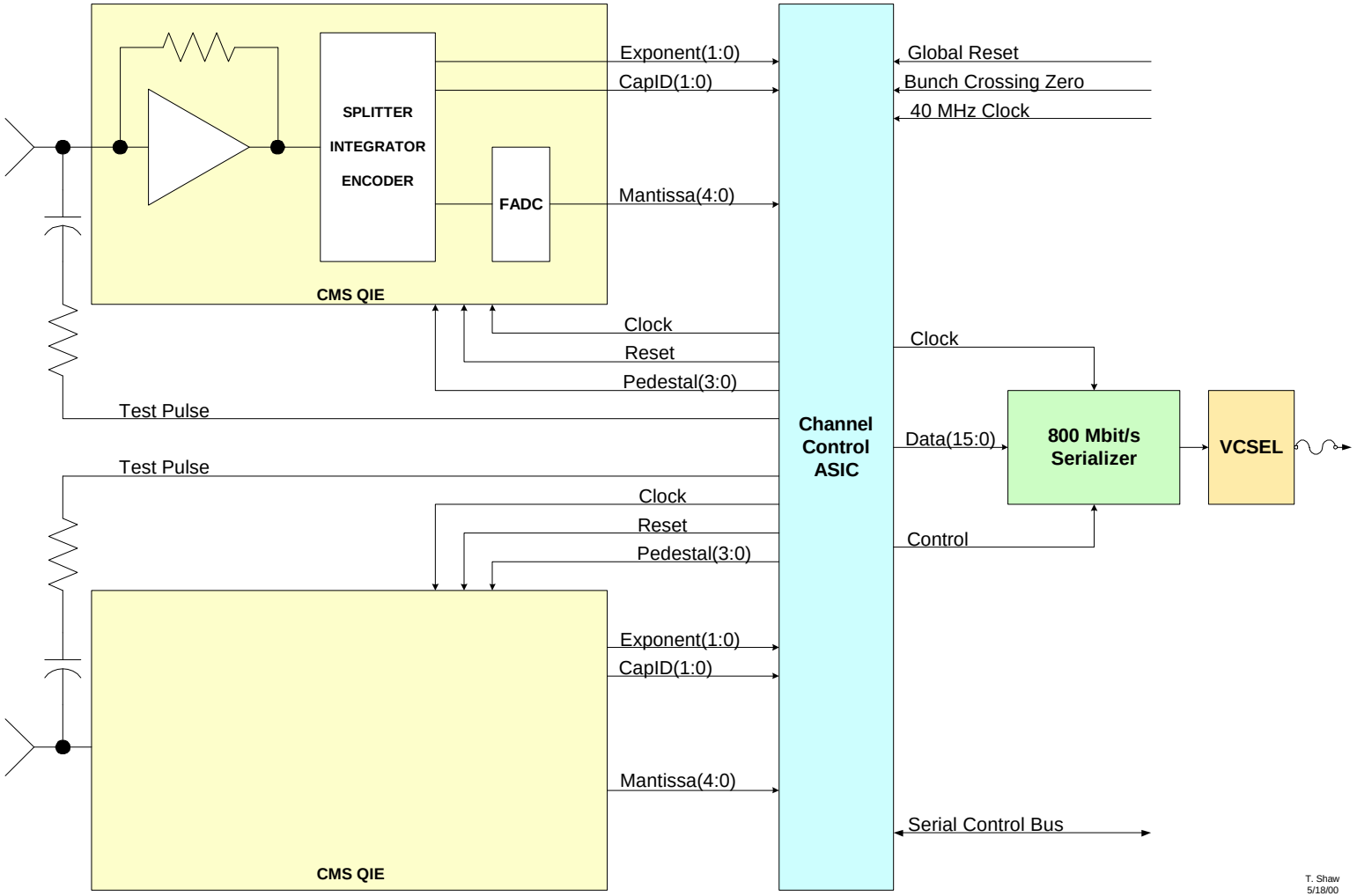
- ~87 CM LONG
- Provides Power
- Distributes 40 MHz Clock (3 load max)
- Provides path for RBXbus (serial communication bus)
- Temperature feedback



Readout Module Overview



FE Channels



CMS QIE Solution

QIE Description

QIE

Charge Integrator Encoder

4 stage pipelined device (25ns per stage)

- charge collection
- settling
- readout
- reset

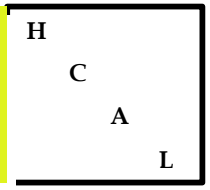
Inverting (HPDs) and Non-inverting (PMTs) Inputs

Internal non-linear Flash ADC

Outputs

- 5 bit mantissa
- 2 bit range exponent
- 2 bit Cap ID

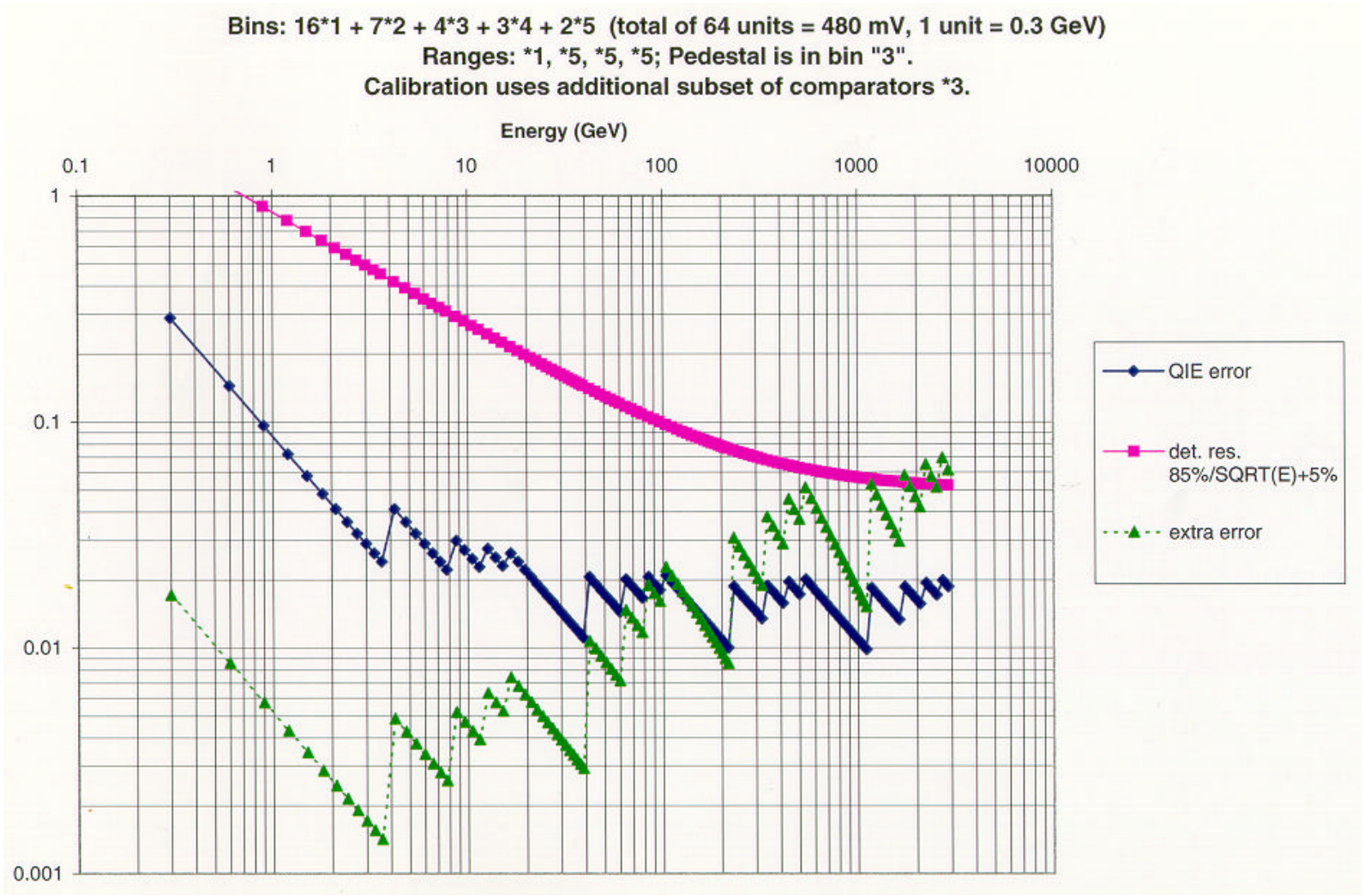
QIE Specification



QIE Design Specifications

- Clock > 40 MHz
- Must accept both polarities of charge
- Charge sensitivity of lowest range – 1fC/LSB
  - In Calibration Mode 1/3 fC/LSB
- Maximum Charge – 9670 fC/25ns
- 4500 electrons rms noise
- FADC Differential Non-Linearity < .05 LSBs

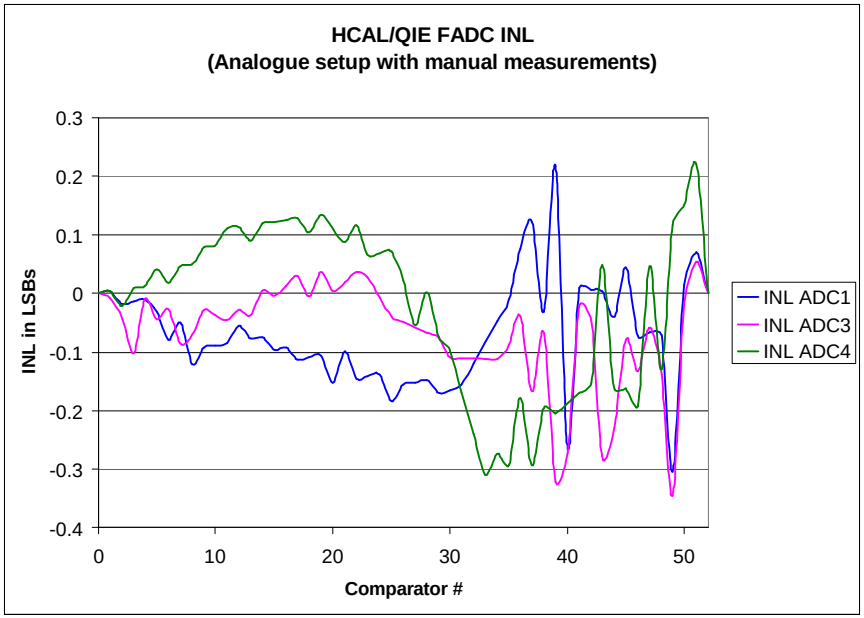
FLASH ADC Quantization

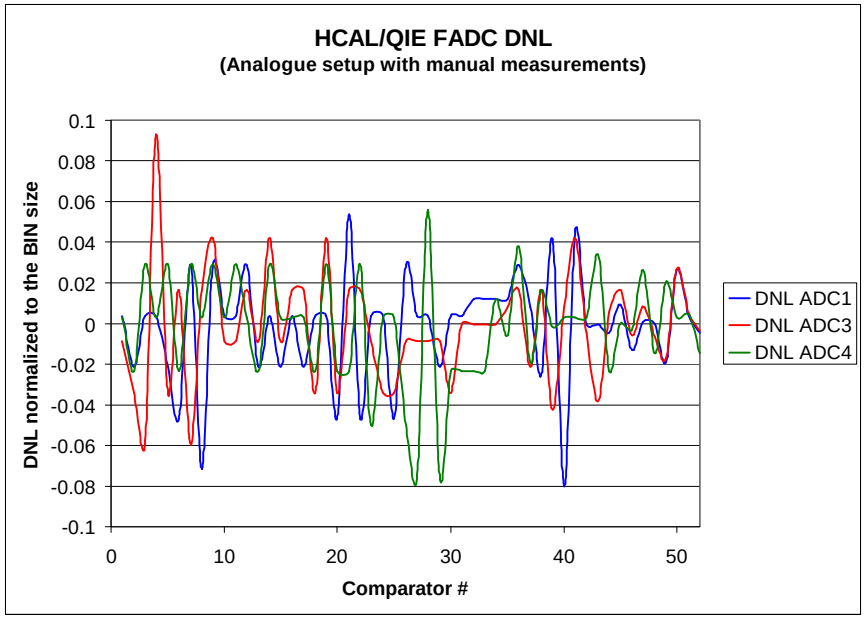


QIE Status

QIE ASIC

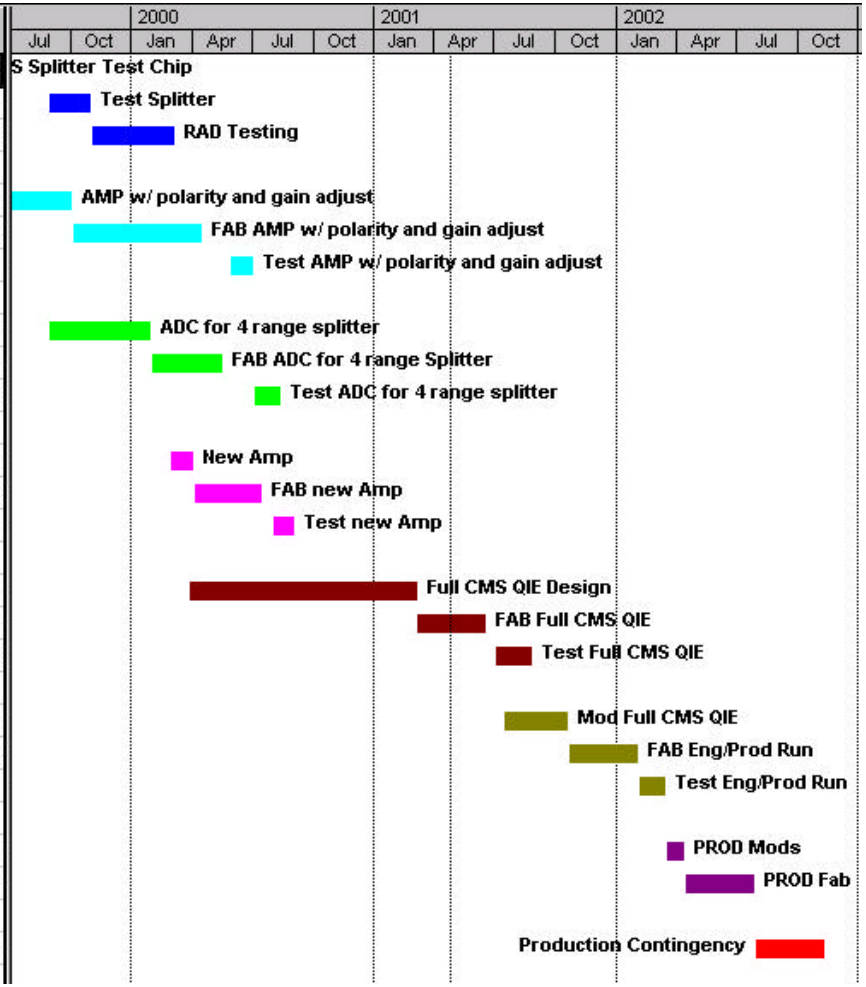
- Current splitter design submitted and tested
- Input amplifier with polarity and gain adjust submitted and tested
- Non-linear Flash ADC design submitted and tested
- Full design submitted – back mid to late June ‘01





QIE Schedule

Task Name	Start	Finish	Duration
AMS splitter test chip	Mon 11/2/98	Fri 4/30/99	130 days
Test Splitter	Mon 8/30/99	Fri 10/29/99	45 days
RAD Testing	Mon 11/1/99	Fri 3/3/00	90 days
AMP w/ polarity and gain adjust	Mon 6/28/99	Fri 10/1/99	70 days
FAB AMP w/ polarity and gain adjus	Mon 10/4/99	Fri 4/14/00	140 days
Test AMP w/ polarity and gain adjus	Mon 5/29/00	Fri 6/30/00	25 days
ADC for 4 range splitter	Mon 8/30/99	Fri 1/28/00	110 days
FAB ADC for 4 range Splitter	Tue 2/1/00	Mon 5/15/00	75 days
Test ADC for 4 range splitter	Mon 7/3/00	Fri 8/11/00	30 days
New Amp	Mon 2/28/00	Fri 3/31/00	25 days
FAB new Amp	Mon 4/3/00	Fri 7/14/00	75 days
Test new Amp	Mon 7/31/00	Fri 9/1/00	25 days
Full CMS QIE Design	Mon 3/27/00	Mon 3/5/01	246 days
FAB Full CMS QIE	Mon 3/5/01	Fri 6/15/01	75 days
Test Full CMS QIE	Mon 7/2/01	Fri 8/24/01	40 days
Mod Full CMS QIE	Mon 7/16/01	Fri 10/19/01	70 days
FAB Eng/Prod Run	Mon 10/22/01	Fri 2/1/02	75 days
Test Eng/Prod Run	Mon 2/4/02	Fri 3/15/02	30 days
PROD Mods	Mon 3/18/02	Fri 4/12/02	20 days
PROD Fab	Mon 4/15/02	Fri 7/26/02	75 days
Production Contingency	Mon 7/29/02	Fri 11/8/02	75 days



Channel Control ASIC

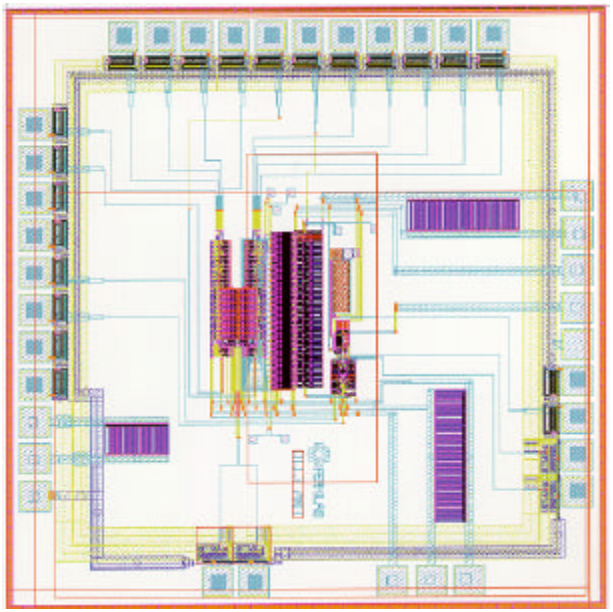
The CCA provides the following functions:

- The processing and synchronization of data from two QIEs,
- The provision of phase-adjusted QIE clocking signals to run the QIE charge integrator and Flash ADC,
- Checking of the accuracy of the Capacitor IDs, the Cap IDs from different QIEs should be in synchronization,
- The ability to force the QIE to use a given range,
- The ability to set Pedestal DAC values,
- The ability to issue a test pulse trigger,
- The provision of event synchronization checks – a crossing counter will be implemented and checked for accuracy with every beam turn marker,
- The ability to send a known pattern to the serial optic link,
- The ability to “reset” the QIE at a known and determined time,
- And, the ability to send and report on any detected errors at a known and determined time.

CCA Status

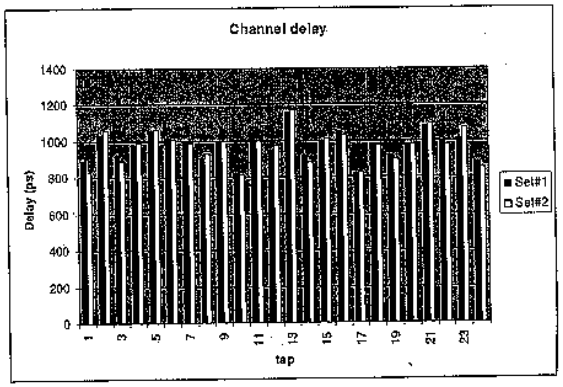
Channel Control ASIC

- DLL for timing control submitted and tested
- 1ns multiplexer design submitted and tested
- Serial Interface design submitted and tested



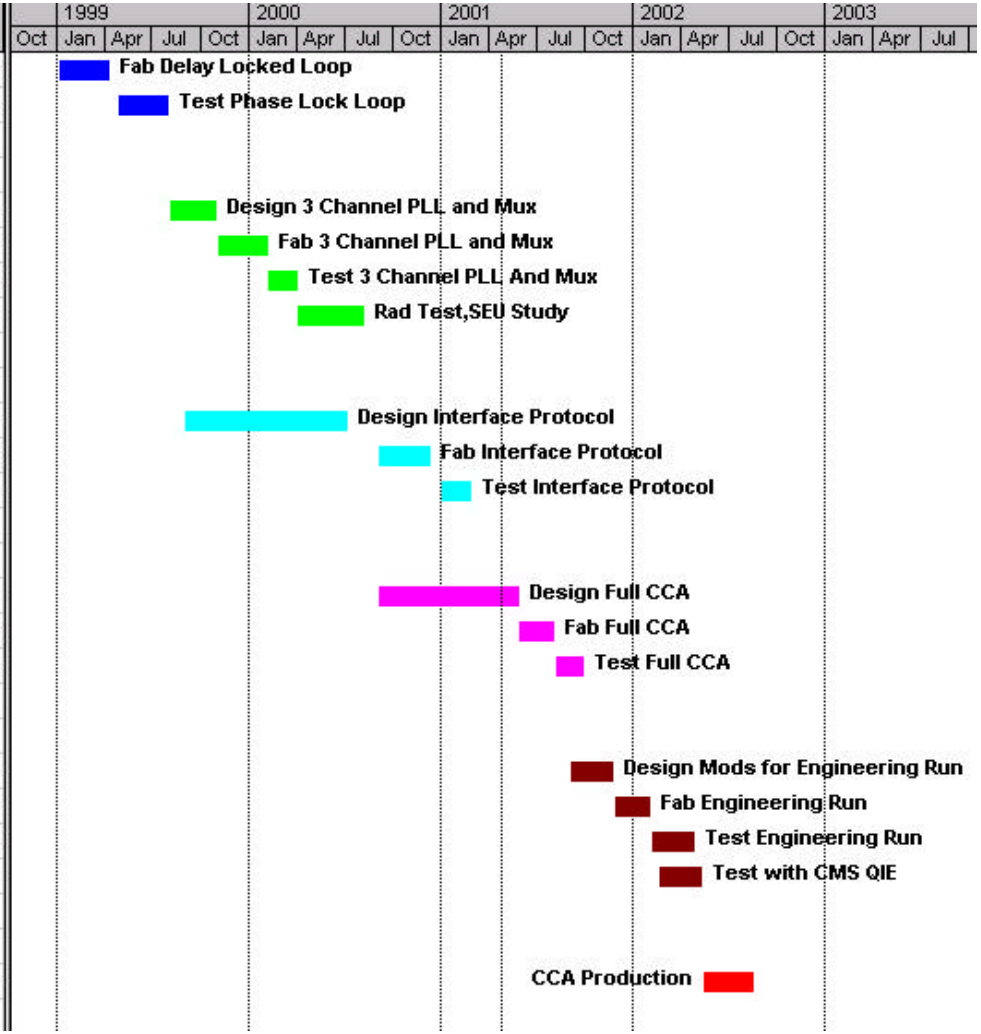
Measured delays vs. tap

- Average delay : 972p STD : 77ps
- Min delay : 810p
- Max delay : 1170p



CCA Schedule

Task Name	Start	Finish	Duration
Fab Phase Locked Loop	Mon 1/4/99	Fri 4/9/99	70 days
Test Phase Lock Loop	Mon 4/26/99	Fri 7/30/99	70 days
Design 3 Channel PLL and	Mon 8/2/99	Fri 10/29/99	65 days
Fab 3 Channel PLL and Mu	Mon 11/1/99	Fri 2/4/00	70 days
Test 3 Channel PLL And M	Mon 2/7/00	Fri 3/31/00	40 days
Rad Test, SEU Study	Mon 4/3/00	Fri 8/4/00	90 days
Design Interface Protocol	Tue 8/31/99	Mon 7/3/00	220 days
Fab Interface Protocol	Mon 9/4/00	Fri 12/8/00	70 days
Test Interface Protocol	Mon 1/1/01	Fri 2/23/01	40 days
Design Full CCA	Mon 9/4/00	Fri 5/25/01	190 days
Fab Full CCA	Mon 5/28/01	Fri 8/3/01	50 days
Test Full CCA	Mon 8/6/01	Fri 9/28/01	40 days
Design Mods for Engineeri	Mon 9/3/01	Fri 11/23/01	60 days
Fab Engineering Run	Mon 11/26/01	Fri 2/1/02	50 days
Test Engineering Run	Mon 2/4/02	Fri 4/26/02	60 days
Test with CMS QIE	Mon 2/18/02	Fri 5/10/02	60 days
CCA Production	Mon 5/13/02	Fri 8/16/02	70 days



GOL Design Specifications

Synchronous (constant latency)

Transmission speed

- **fast: 1.6 Gbps , 32 bit data input @ 40 MHz**
- **slow: 0.8 Gbps , 16 bit data input @ 40 MHz**

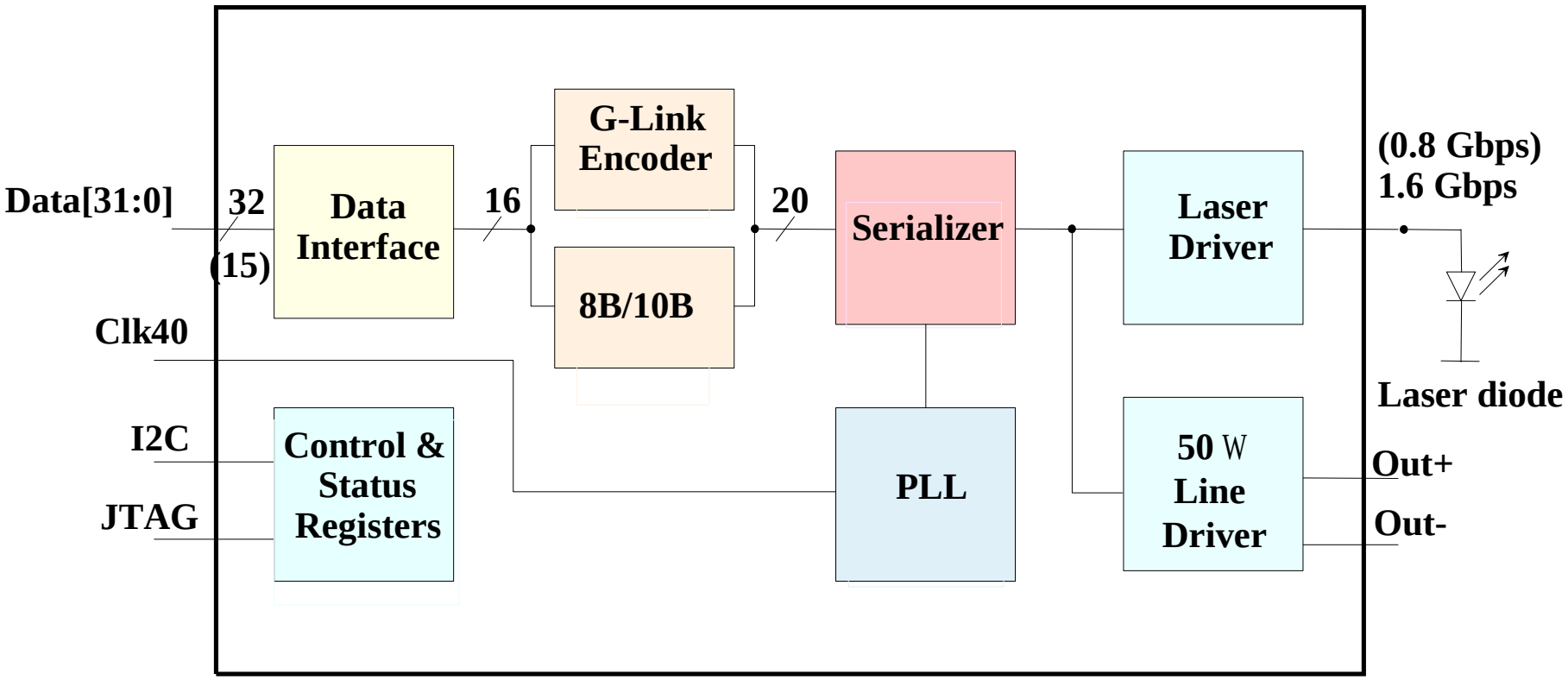
Two encoding schemes

- **G-Link**
- **Fiber channel (8B/10B)**

Interfaces for control and status registers

- **I2C**
- **JTAG**

Gigabit link (G-Link, 8B/10B optional)



GOL Radiation hardness

Deep submicron (0.25 um) CMOS

Enclosed CMOS transistors

Triple voting in state machines

Up-sizing of PLL components

Auto-error correction in Config. registers

Single Event Upsets

- Can we extrapolate for LHC?

CMS Environment	Pixel R = 4 – 20cm	Endcap ECAL R = 50 – 130cm	Tracker R = 65-120cm	Cavern R = 700 – 1200cm
Error/(chip hour)	$1.4\ 10^{-2}$	$1.9\ 10^{-4}$	$8.4\ 10^{-5}$	$3.1\ 10^{-8}$
#chips for one error each hour!	71	5.3K	12K	32M

GOL Status

- **Bit error rate test in the 800Mbit/s G-Link mode: 20 hours error free transmission (external laser driver).**
- **Bit error rate test in the 1.6Gbit/s 8B/10B mode: 13 hours error free transmission (external laser driver).**
- **I2C interface successfully tested.**
- **JTAG interface successfully tested.**

- **Need to understand and fix jitter problem on internal laser driver. This will be fixed in the next submission (April '01).**

VCSEL Selection

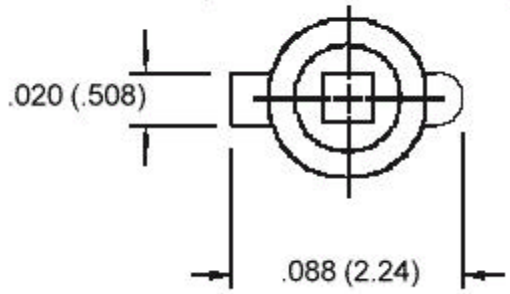
HFE4086-001

VCSEL Components, Data Communications, Flat Window Pillpack, Unattenuate optics, no back monitor photodiode

FEATURES

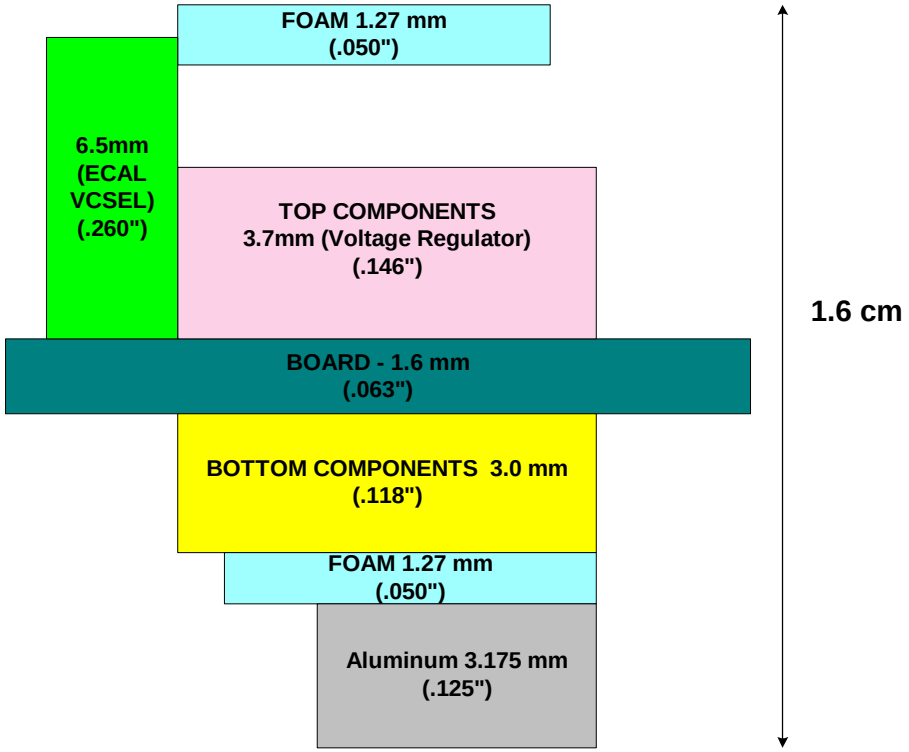
- Designed for drive currents between 5 mA and 15 mA
- Optimized for low dependence of electrical properties over temperature
- High speed > 1 Ghz
- Miniature flat-window, pill-pack package

MOUNTING DIMENSIONS (for reference only): in./(mm)



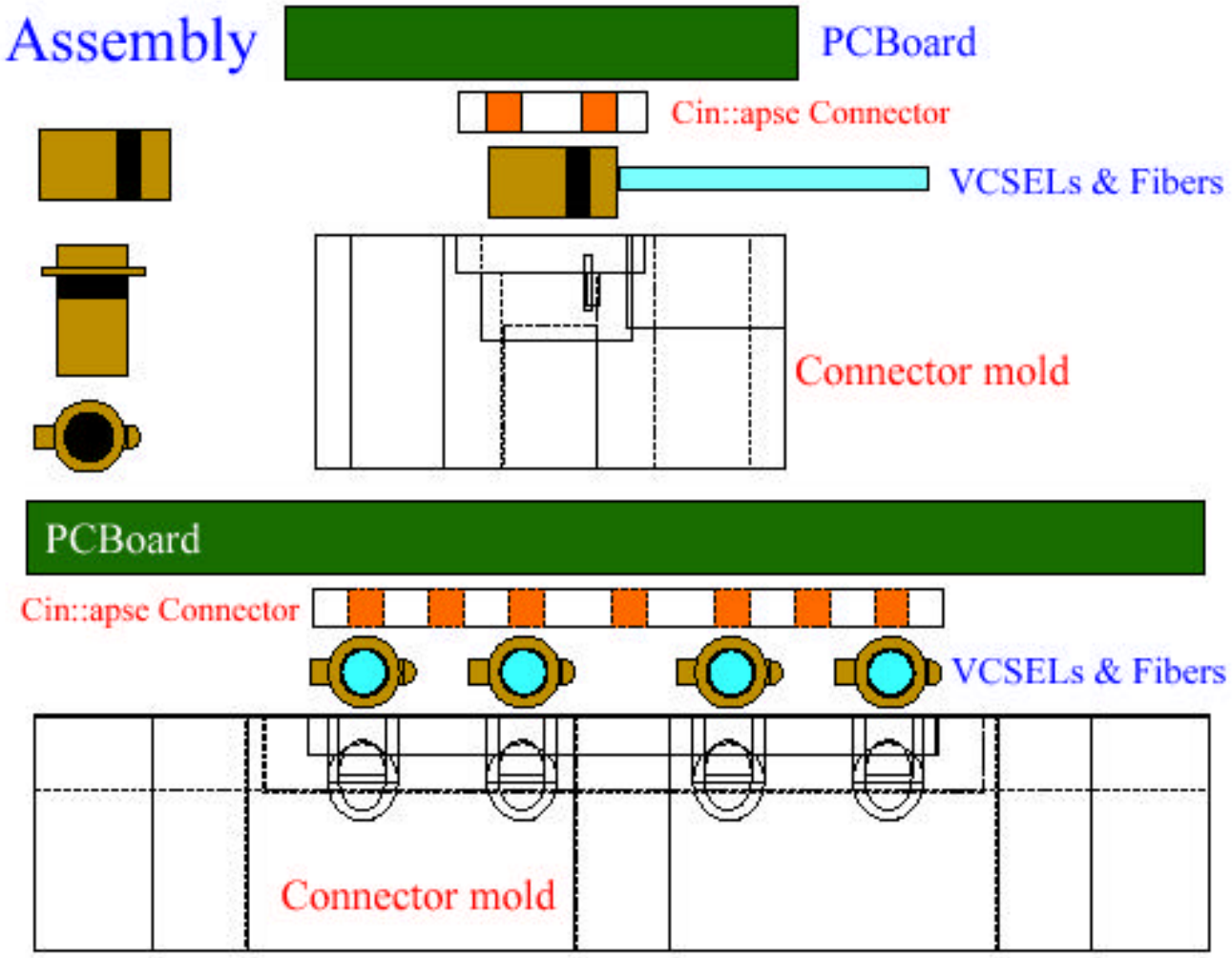
Readout Card Component Height

Goal is 1.6 cm stack



Geometric Space For Components

VCSEL Mechanics



Rad Tolerant Voltage Regulator

Developed by ST Microelectronics

Specified by CERN RD49

Shown to be Rad Hard

Presently fixing overvoltage protection

Pre-production parts due June 2001

Production parts late 2001

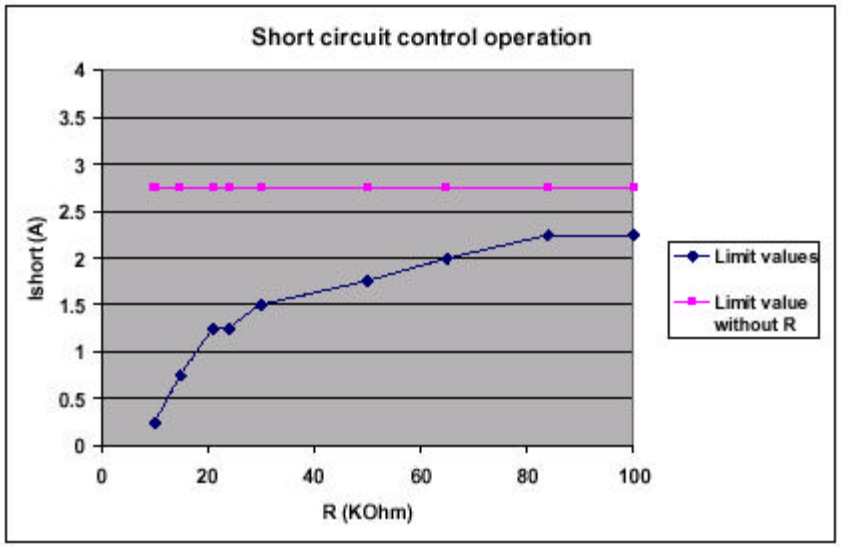


Fig. 7: Tuning of the maximum output current in a 2nd edition prototype regulator (version 2.5 V).

Production Phase

H C A L

What we need to make it all work

- HPDs and Interface Cards
- ODU Assemblies
- RBXs
- Electrical Backplanes
- HV distributors
- Readout Modules
- FE Cards
  - QIEs
  - CCAs
  - GOLs
  - Voltage Regulators
  - VCSELs

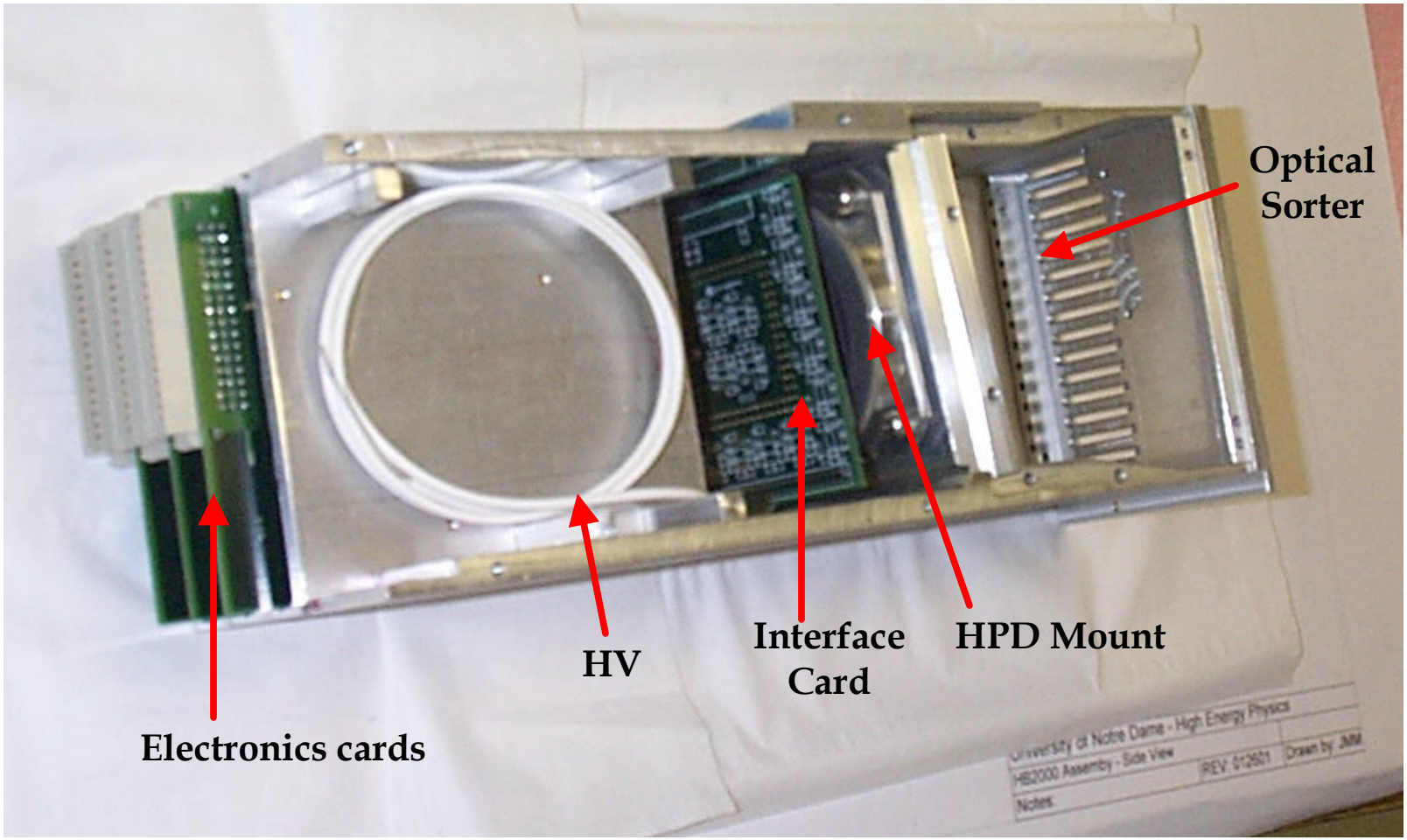
HB RBX Assembly

Full RBX with 19 ch RMs

RBX Interior -- HV distributor and backplane

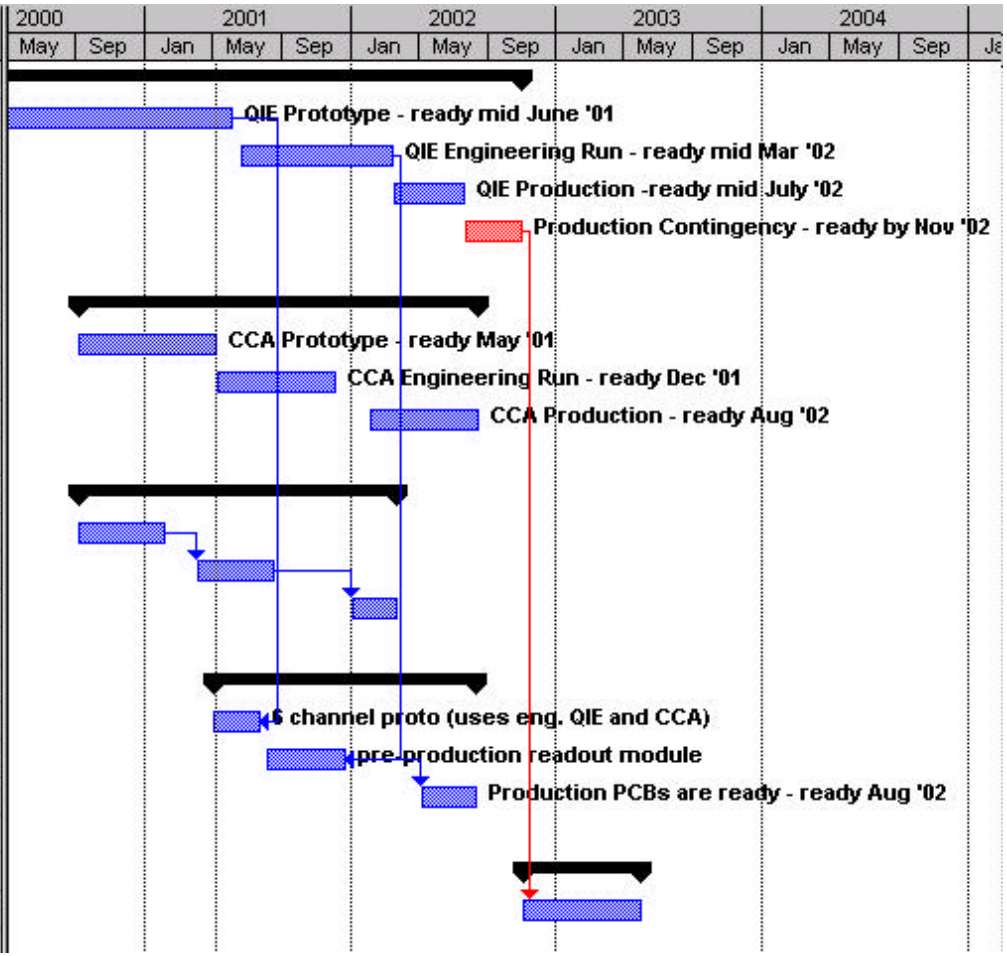
RM19 Sidewall removed

- **The readout module (RM) integrates the HPD, front end electronics, and digital optical drivers.**



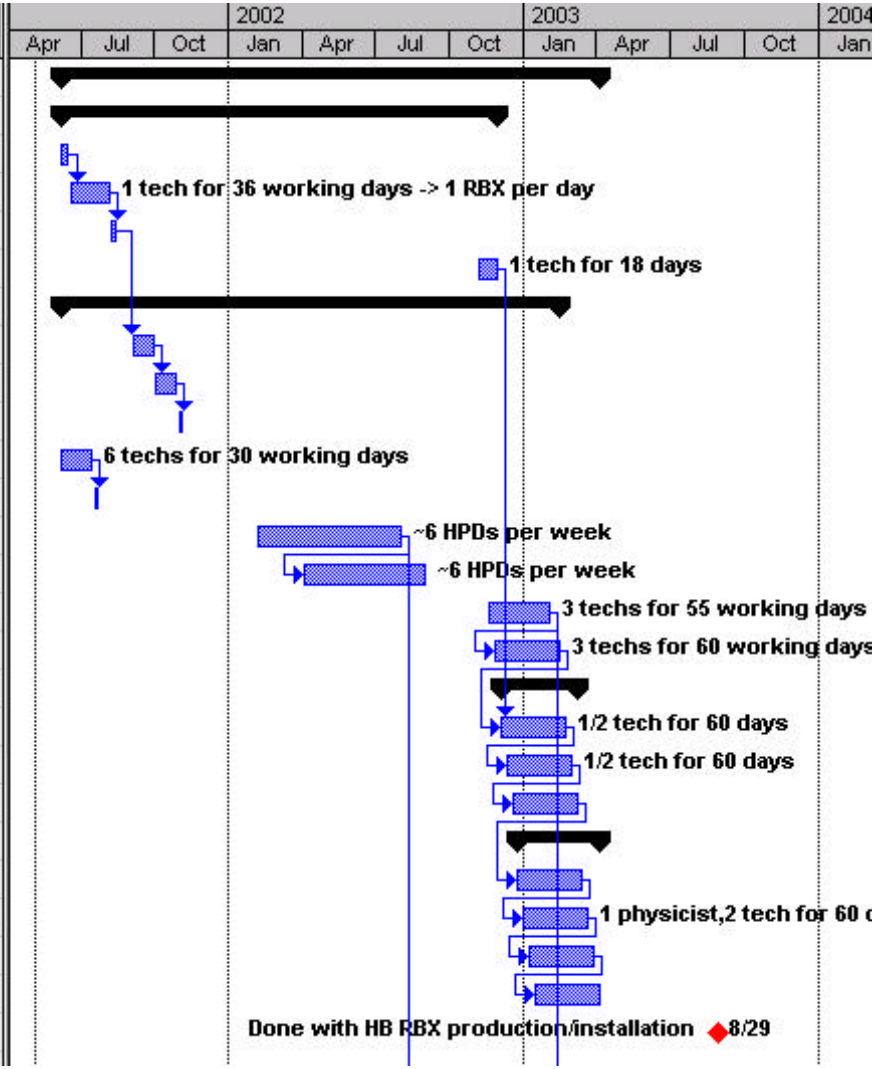
Electronics Development

Task Name	Start	Finish
QIE ASIC	**Mon 3/13/00**	**Thu 10/31/02**
QIE Prototype	Mon 3/13/00	Mon 6/4/01
QIE Engineering Run	Mon 6/18/01	Fri 3/15/02
QIE Production	Mon 3/18/02	Mon 7/22/02
QIE Contingency	Mon 7/22/02	Thu 10/31/02
Channel Control ASIC	**Mon 9/4/00**	**Fri 8/16/02**
CCA Prototype	Mon 9/4/00	Mon 5/7/01
CCA Engineering Run	Mon 5/7/01	Mon 12/3/01
CCA Production	Mon 2/4/02	Fri 8/16/02
Optical TX	**Mon 9/4/00**	**Mon 3/25/02**
TX Design	Mon 9/4/00	Mon 2/5/01
TX Engineering Run	Mon 4/2/01	Fri 8/17/01
TX Production - Delivery	Tue 1/1/02	Mon 3/25/02
6 Channel Readout Module	**Tue 5/1/01**	**Mon 8/12/02**
Proto Readout Card	Tue 5/1/01	Mon 7/23/01
Pre-Production Readout Card	Mon 8/6/01	Fri 12/21/01
Production Readout PCB's	Mon 5/6/02	Mon 8/12/02
Electronics Installation	**Fri 11/1/02**	**Fri 5/30/03**
6 Channel Board Assembly	Fri 11/1/02	Fri 5/30/03



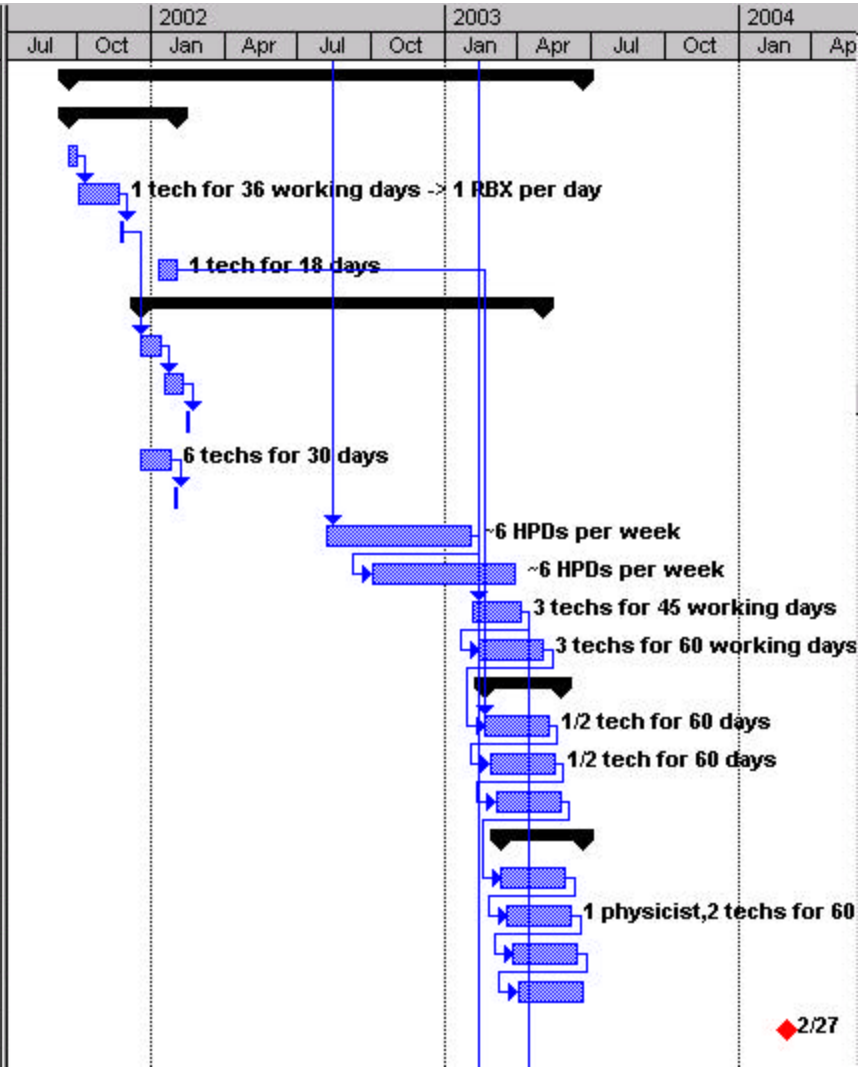
HB RBX Production and Installation

Task Name	Duration	Start	Finish
HB RBX Production/Installation	**480 days**	**Mon 6/4/01**	**Fri 4/4/03**
Produce 36 HB RBXs	**390 days**	**Mon 6/4/01**	**Fri 11/29/02**
Manufacture HB Readout Boxes (RBX)	10 days	Mon 6/4/01	Fri 6/15/01
Assemble HB RBXs	36 days	Mon 6/18/01	Mon 8/6/01
Ship HB RBXs to FNAL	5 days	Tue 8/7/01	Mon 8/13/01
Install Backplanes in HB RBXs	20 days	Mon 11/4/02	Fri 11/29/02
Produce 180 Readout Modules	**445 days**	**Mon 6/4/01**	**Fri 2/14/03**
Manufacture 144 RM-19 Parts	20 days	Mon 9/3/01	Fri 9/28/01
Manufacture 36 RM-73 Parts	20 days	Mon 10/1/01	Fri 10/26/01
Ship RM parts to FNAL	5 days	Mon 10/29/01	Fri 11/2/01
Assemble Optical Decoder Units (ODUs)	30 days	Mon 6/4/01	Fri 7/13/01
Ship ODUs to FNAL	5 days	Mon 7/16/01	Fri 7/20/01
Test Hybrid Photodetectors (HPDs)	130 days	Mon 2/4/02	Fri 8/2/02
Ship HPDs to Fermilab	110 days	Mon 4/1/02	Fri 8/30/02
Checkout Front end electronics modules	55 days	Mon 11/18/02	Fri 1/31/03
Assemble 180 RMs	60 days	Mon 11/25/02	Fri 2/14/03
RBX Integration at FNAL	**70 days**	**Mon 12/2/02**	**Fri 3/7/03**
Install/Checkout RMs in RBX	60 days	Mon 12/2/02	Fri 2/21/03
Burn-in RBXs	60 days	Mon 12/9/02	Fri 2/28/03
Ship RBXs to CERN	60 days	Mon 12/16/02	Fri 3/7/03
RBX Integration at CERN	**75 days**	**Mon 12/23/02**	**Fri 4/4/03**
Receive RBXs	60 days	Mon 12/23/02	Fri 3/14/03
Test RBXs	60 days	Mon 12/30/02	Fri 3/21/03
Install and Cable RBXs	60 days	Mon 1/6/03	Fri 3/28/03
Test Installed RBX	60 days	Mon 1/13/03	Fri 4/4/03
GOAL is to be done with HB by end of Aug'03	1 day	Fri 8/29/03	Fri 8/29/03



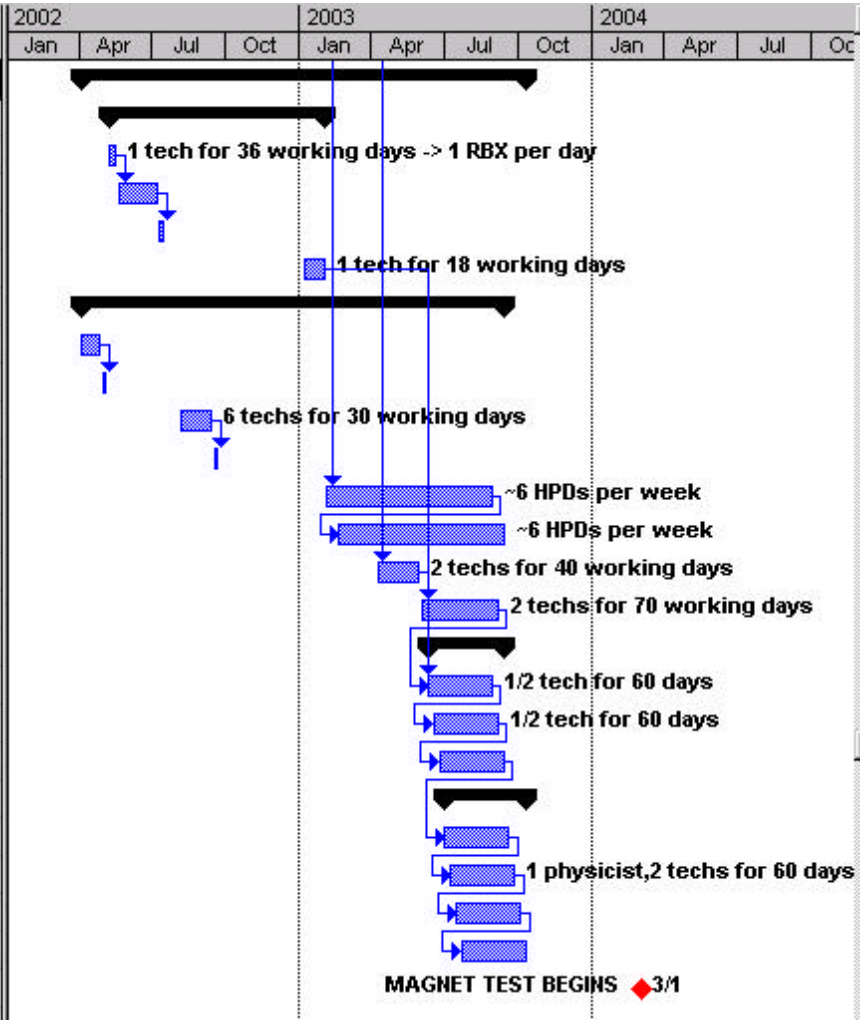
HE RBX Production and Installation

Task Name	Duration	Start	Finish
HE RBX Production/Installation	**460 days**	**Mon 9/17/01**	**Fri 6/20/03**
Produce 36 HE RBXs	**100 days**	**Mon 9/17/01**	**Fri 2/1/02**
Manufacture HE Readout Boxes (RBX)	10 days	Mon 9/17/01	Fri 9/28/01
Assemble HE RBXs	36 days	Mon 10/1/01	Mon 11/19/01
Ship HE RBXs to FNAL	5 days	Tue 11/20/01	Mon 11/26/01
Install Backplanes in HE RBXs	20 days	Mon 1/7/02	Fri 2/1/02
Produce 180 Readout Modules	**360 days**	**Mon 12/17/01**	**Fri 5/2/03**
Manufacture 144 RM-19 Parts	20 days	Mon 12/17/01	Fri 1/11/02
Manufacture 36 RM-73 Parts	20 days	Mon 1/14/02	Fri 2/8/02
Ship RM parts to FNAL	5 days	Mon 2/11/02	Fri 2/15/02
Assemble Optical Decoder Units (ODUs)	30 days	Mon 12/17/01	Fri 1/25/02
Ship ODUs to FNAL	5 days	Mon 1/28/02	Fri 2/1/02
Test Hybrid Photodetectors (HPDs)	130 days	Mon 8/5/02	Fri 1/31/03
Ship HPDs to Fermilab	130 days	Mon 9/30/02	Fri 3/28/03
Checkout Front end electronics modules	45 days	Mon 2/3/03	Fri 4/4/03
Assemble 180 RMs	60 days	Mon 2/10/03	Fri 5/2/03
RBX Integration at FNAL	**70 days**	**Mon 2/17/03**	**Fri 5/23/03**
Install/Checkout RMs in RBX	60 days	Mon 2/17/03	Fri 5/9/03
Burn-in RBXs	60 days	Mon 2/24/03	Fri 5/16/03
Ship RBXs to CERN	60 days	Mon 3/3/03	Fri 5/23/03
RBX Integration at CERN	**75 days**	**Mon 3/10/03**	**Fri 6/20/03**
Receive RBXs	60 days	Mon 3/10/03	Fri 5/30/03
Test RBXs	60 days	Mon 3/17/03	Fri 6/6/03
Install and Cable RBXs	60 days	Mon 3/24/03	Fri 6/13/03
Test Installed RBX	60 days	Mon 3/31/03	Fri 6/20/03
GOAL is to be done with HE by end of Feb'04	1 day	Fri 2/27/04	Fri 2/27/04

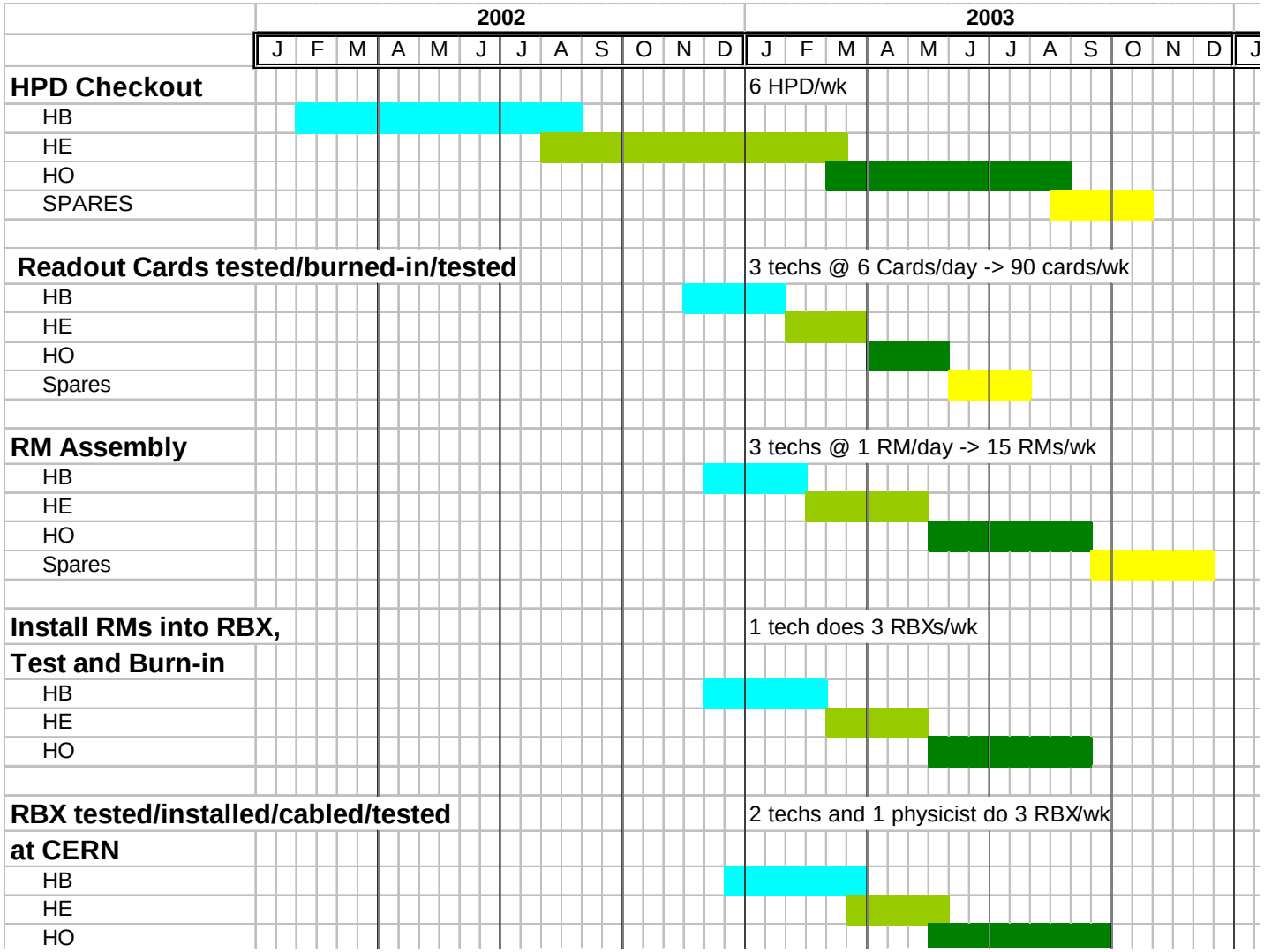


HO RBX Production and Installation

Task Name	Duration	Start	Finish
HO RBX Production/Installation	**400 days**	**Mon 4/1/02**	**Fri 10/10/0**
Produce 36 HO RBXs	**195 days**	**Mon 5/6/02**	**Fri 1/31/03**
Manufacture HO Readout Boxes (RBX)	10 days	Mon 5/6/02	Fri 5/17/02
Assemble HO RBXs	36 days	Mon 5/20/02	Mon 7/8/02
Ship HO RBXs to FNAL	5 days	Tue 7/9/02	Mon 7/15/02
Install Backplanes in HO RBXs	20 days	Mon 1/6/03	Fri 1/31/03
Produce 140 Readout Modules	**380 days**	**Mon 4/1/02**	**Fri 9/12/03**
Manufacture 140 RM-19 Parts	20 days	Mon 4/1/02	Fri 4/26/02
Ship RM parts to FNAL	5 days	Mon 4/29/02	Fri 5/3/02
Assemble Optical Decoder Units (ODUs)	30 days	Mon 8/5/02	Fri 9/13/02
Ship ODUs to FNAL	5 days	Mon 9/16/02	Fri 9/20/02
Test Hybrid Photodetectors (HPDs)	150 days	Mon 2/3/03	Fri 8/29/03
Ship HPDs to Fermilab	150 days	Mon 2/17/03	Fri 9/12/03
Checkout Front end electronics modules	40 days	Mon 4/7/03	Fri 5/30/03
Assemble 140 RMs	70 days	Mon 6/2/03	Fri 9/5/03
RBX Integration at FNAL	**70 days**	**Mon 6/9/03**	**Fri 9/12/03**
Install/Checkout RMs in RBX	60 days	Mon 6/9/03	Fri 8/29/03
Burn-in RBXs	60 days	Mon 6/16/03	Fri 9/5/03
Ship RBXs to CERN	60 days	Mon 6/23/03	Fri 9/12/03
RBX Integration at CERN	**75 days**	**Mon 6/30/03**	**Fri 10/10/03**
Receive RBXs	60 days	Mon 6/30/03	Fri 9/19/03
Test RBXs	60 days	Mon 7/7/03	Fri 9/26/03
Install and Cable RBXs	60 days	Mon 7/14/03	Fri 10/3/03
Test Installed RBX	60 days	Mon 7/21/03	Fri 10/10/03
GOAL is to be done with HO by end of Feb'04	1 day	Mon 3/1/04	Mon 3/1/04



FE Installation Plan



FE Summary

Prototype ASICs will begin arriving this summer

We have scheduled a vertical slice test for late summer ’01

We have prepared schedules and plans for final assembly and installation